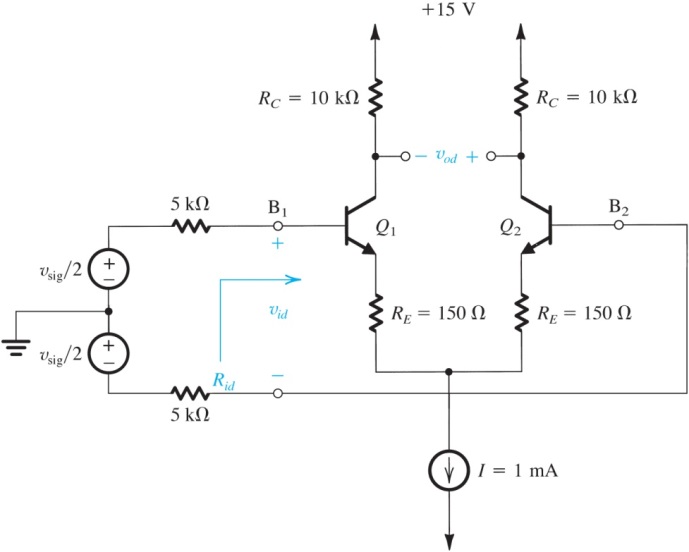
ELEG 312 - Example Problems Chapter 9-2

**Example 9.3**

The differential amplifier in Fig. 9.24 uses transistors with ** = 100. Evaluate the following:

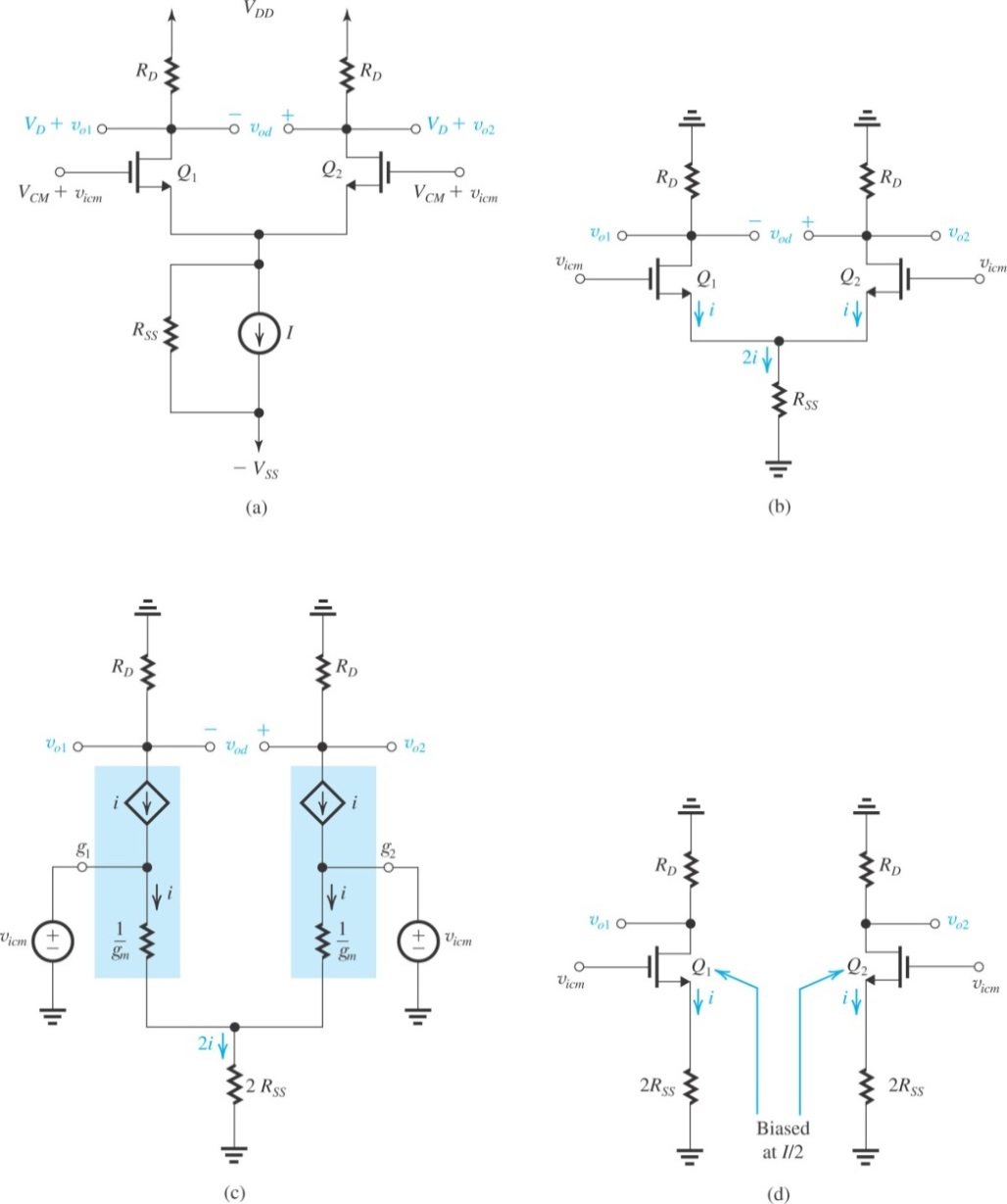
(a) The input differential resistance *Rid.*

(b) The overall differential voltage gain *vod/vsig.* (neglect the effect of *ro*).



**Example 9.4**

In this example we consider the design of the current source that supplies the bias current of a MOS differential amplifier. Let it be required to achieve a CMRR of 100 dB and assume that the only source of mismatch between *Q*1 and *Q*2 is a 2% mismatch in their *W*/L ratios. Let *I* = 200 μA and assume that all transistors are to be operated at *VOV* = 0.2 V. For the 0.18-μm CMOS fabrication process available, *V’A*= 5 V/μm. If a simple current source is utilized for *I*, what channel length is required? If a cascode current source is utilized, what channel length is needed for the two transistors in the cascode?



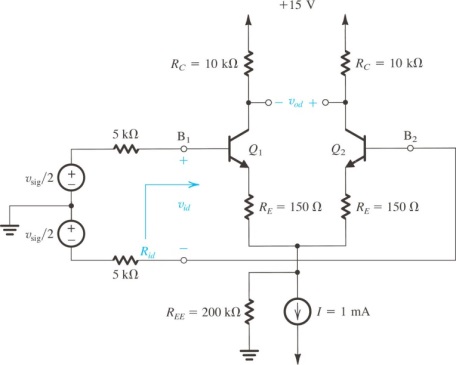
**Example 9.5**

For the differential amplifier analyzed in Example 9.3, let the bias-current source have an output resistance *REE*= 200 k. Evaluate:

(a) the worst-case common-mode gain if the two collector resistances are accurate to within ±1%.

(b) the CMRR in dB.

(c) the input common-mode resistance (assuming the Early voltage *VA* = 100 V).



**Exercise 9.15**

For the MOS differential pair specified in Exercise 9.4, find the three components of the input offset voltage. Let *RD*/*RD* = 2%,  (*W*/*L*)/(*W*/*L*)= 2%, and *Vt* = 2 mV. Use Eq. (9.110) to obtain an estimate of the total *VOS*.

**Exercise 9.16**

For a BJT differential amplifier utilizing transistors having β = 100, matched to 10% or better, and areas that are matched to 10% or better, along with collector resistors that are matched to 2% or better, find *VOS*, *IB*, and *IOS*. The dc bias current *I* is 100 μA.